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HMC240

GaAs MMIC SPDT SWITCH DC - 4.0 GHz

Typical Applications

The HMC240 is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation

Features

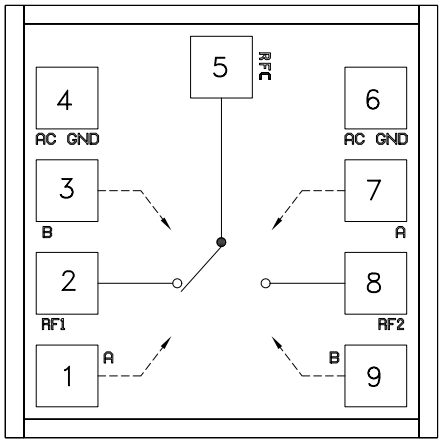
Broadband Performance: DC - 4.0 GHz

Low Insertion Loss: 0.5 dB @ 2.0 GHz

High IIP3: +48 dBm

Small Size: 0.70 mm x 0.70 mm x 0.13 mm

Functional Diagram



Pads 3 & 7 are alternate A & B Control Inputs.

General Description

The HMC240 is a low cost GaAs MESFET SPDT switch chip. Covering DC to 4.0 GHz, this switch offers high isolation and low insertion loss. RF1 and RF2 are reflective shorts when “off”. The switch can operate using either two negative control logic inputs of -5/0V or two positive control voltage logic inputs of 0/+5V. All data is tested with the chip in a 50 Ohm test fixture connected via 0.025 mm (1 mil) diameter wire bonds of 0.31 mm (12 mils) length.

Electrical Specifications, T_A = +25° C, With 0/-5V Control or +5/0V Control, 50 Ohm System

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 3.0 GHz DC - 4.0 GHz		0.4 0.5 0.6 0.9	0.7 0.8 0.9 1.4	dB dB dB dB
Isolation	DC - 4.0 GHz	24	28		dB
Return Loss “On State”	DC - 1.0 GHz DC - 2.0 GHz DC - 3.0 GHz DC - 4.0 GHz		22 16 14 11		dB dB dB dB
Input Power for 1 dB Compression	0.5 - 1.0 GHz 0.5 - 4.0 GHz	25 23	30 29		dBm dBm
Input Third Order Intercept (Two-Tone Input Power= +7 dBm Each Tone)	0.5 - 1.0 GHz 0.5 - 4.0 GHz	43 40	48 45		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 4.0 GHz		 3 10		 ns ns

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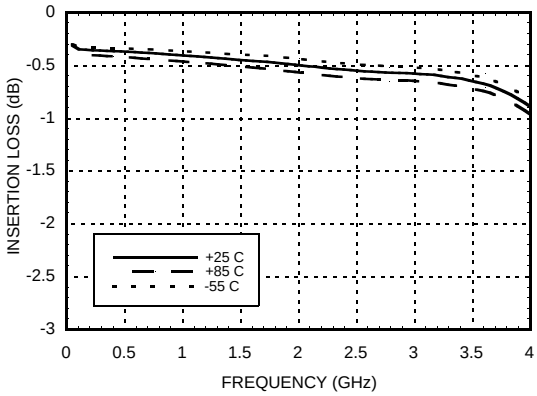
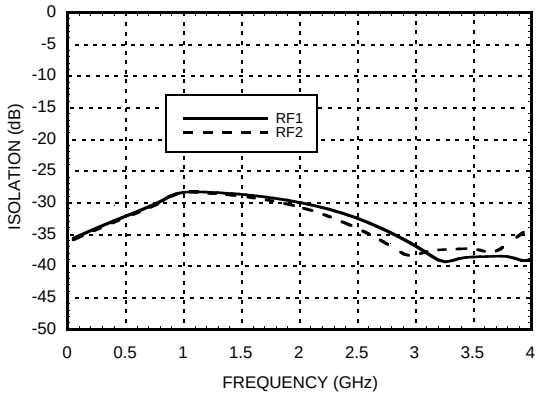
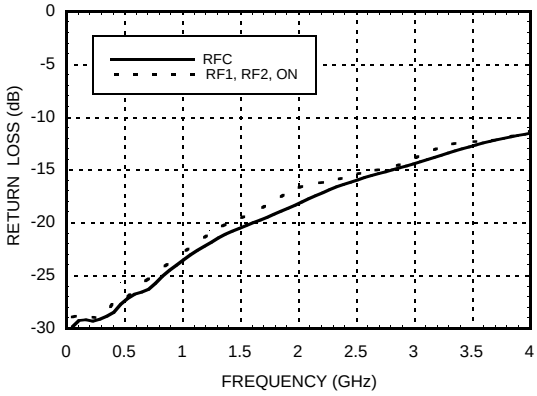
Insertion Loss vs. Temperature



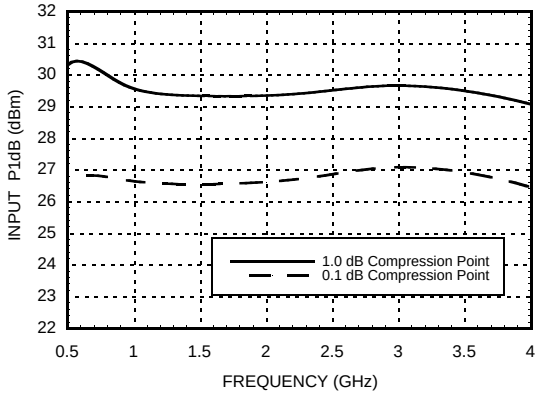
Isolation



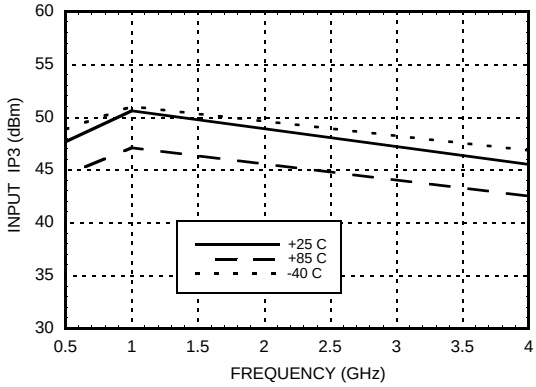
Return Loss



0.1 and 1 dB Input Compression Point



Input Third Order Intercept Point



Absolute Maximum Ratings

RF Input Power V_{ctrl}= 0/+5 (-5)V	< 0.5 GHz 0.5 - 4 GHz	+27 dBm +34 dBm
Control Voltage Range (A & B= 0/+5V)		-0.2 to +10 Vdc
Control Voltage Range (A & B= -5/0V)		-10 to +0.2 Vdc
Storage Temperature		-65 to +150 deg C
Operating Temperature		-55 to +85 deg C

Positive Control Voltage

State	Bias Condition
Low	0 Vdc @ 10 uA
High	+3 Vdc @ 10 uA to +8 Vdc @ 70 uA
Control input voltage tolerences are ±0.2 Vdc.	

Negative Control Voltage

State	Bias Condition
Low	-3 Vdc @ 10 uA to -8 Vdc @ 70 uA
High	0 Vdc @ 10 uA
Control input voltage tolerences are ±0.2 Vdc.	

Truth Table: Positive Control Voltage

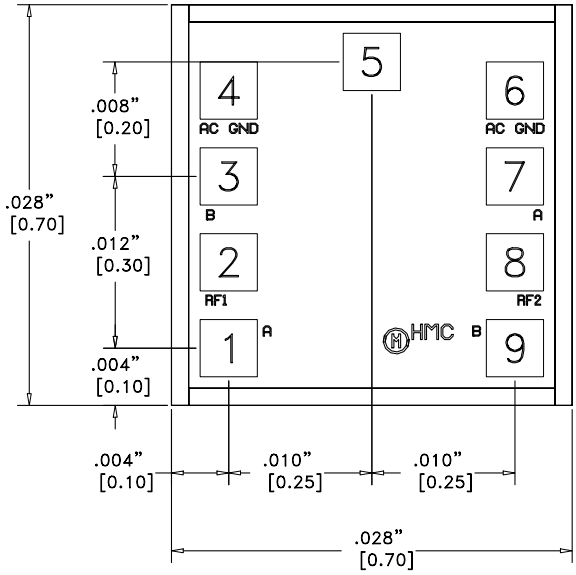
Control Input		Control Current		Signal Path State	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RFC to RF1	RFC to RF2
0	+5	-50	50	ON	OFF
+5	0	50	-50	OFF	ON

Truth Table: Negative Control Voltage

Control Input		Control Current		Signal Path State	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RFC to RF1	RFC to RF2
-5	0	-50	50	ON	OFF
0	-5	50	-50	OFF	ON

Note:
This part can be controlled with either positive or negative voltages per the above table. DC blocks are required at ports RFC, RF1 and RF2 if positive control voltage is used.

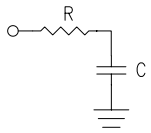
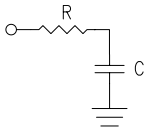
Outline Drawing



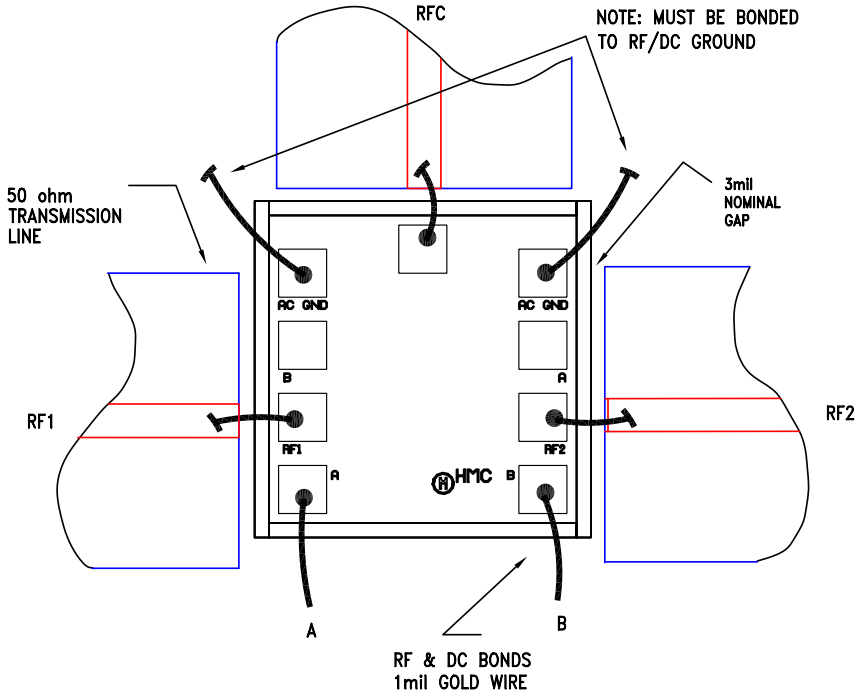
NOTES:

1. DIMENSIONS IN INCHES [MILLIMETERS].
2. DIE THICKNESS IS 0.005".
3. TYPICAL BOND PAD IS 0.004" SQUARE.
4. TYPICAL BOND PAD SPACING IS 0.006" CENTER TO CENTER.
5. BOND PAD METALLIZATION: GOLD.
6. PADS 4 AND 6 MUST BE CONNECTED TO RF/DC GROUND.

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 7	A, A (alt.)	See truth table and control voltage table. Connect either pad 1 or pad 7 to control logic input.	
2, 5, 8	RF1, RFC, RF2	These pads are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
3, 9	B, B (alt.)	See truth table and control voltage table. Connect either pad 3 or pad 9 to control logic input.	
4, 6	AC GND	Must be connected to RF/DC ground.	

Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).

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